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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/334,354
Filing Date: June 16, 1999
Appellant(s): TAJIME ET AL.

Ian R. Blum
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed September 28, 2005 appealing from the Office action mailed April 1, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

It is to be noted that a typo exists in the heading. "Objection" as shown in the section VI heading of page 8 of the Brief should be "Rejection" instead.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-14 and 16-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohira et al of record (6,208,689).

The Examiner wants to point out that the claimed limitations that constitute as new matter (see above paragraph (2)) have not been considered in the following art rejections.

Ohira et al discloses a method and apparatus for digital image decoding as shown in Figures 18, 19, 24, 29, 30, 49-53, and the same moving picture decoding method and apparatus as claimed in claims 1-14 and 16-18, comprising the same compressor (i.e., 107a of Figures 18 and 24, 112a of Figure 49, see 107b of Figures 29 and 30) that compresses a decoded image and stores the resulting compressed image in a memory (i.e., 103 of Figures 18 and 49); an expander (i.e., see 108, 109 of Figure 18; 113a, 114a of Figure 49) that expands a compressed image stored in the memory; a quantization controller (see Figures 18, 19, 24, 29, 30, 50-52, column 13, line 61 to column 14, line 64, column 15, line 56 to column 16, line 45, column 24, line 37 to column 25, line 12) that controls how quantization is performed in the compressor; a memory access width controller (i.e., as provided by compression rate judging section 106 of Figure 18 since compression rate judging section 106 provides the rate of compression in connection with

the storage capacity, i.e. number of bits of the memory 103, and bit allocation control to the quantization controller is being provided within 107a of Figures 18, 24, 107b of Figures 29, 39, and 112a of Figures 49 and 50, see Figures 18, 24, 29, 30, 49-52, column 13, lines 16-44, column 14, lines 3-64, column 17, line 33 to column 19, line 13) that controls the quantization controller such that bit allocation is controlled in relation to the number of bits of a memory access unit of the memory, the memory access width controller controls the quantization controller such that a number of coded bits of the image processed in the compressor for every control unit of compression processing is in conformity with the number of bits of the memory access unit of the memory in the case that the coded number of bits exceeds the number of bits of the memory access unit of the memory, the memory access width controller conducts control using information included in the compressed stream, the memory access width controller applies control to the quantization controller such that when an allocated number of bits of coded data of a compression block exceeds the number of bits of the memory access unit of the memory or is less than the number of bits of the memory access unit of the memory, the allocated number of bits is made equal to or less than the number of bits of the memory access unit of the memory by subtracting a predetermined number of bits from the allocated bits of coded data of the compression processing block or by increasing the number of allocated bits by the predetermined number of bits, whereby the coded data is enabled to be extracted from the memory with one access occurrence (i.e., data in the compressing section 107a of Figure 18 are compressed based upon the compression rate information 157 from the compression rate judging section 106, the compression rate judging section selects a compression mode from among a plurality of compression modes based upon the rate of compression, thereby providing the increase/decrease

in the number of bits allocated and providing the rate of compression in connection with the memory, i.e. number of bits, of the memory 103, and bit allocation control to the quantization controller is being provided within 107a of Figures 18, 24, 107b of Figures 29, 39, and 112a of Figures 49 and 50, and see column 13, lines 16-44, column 14, lines 3-64, column 17, line 33 to column 19, line 13); the quantization controller controls quantization performed by the compressor based on access width information from the memory access width controller such that a number of bits processed in the compressor for every control unit of compression processing is equal to or less than the number of bits of the memory access unit of the memory in the case that the number of bits for every control unit of compression processing exceeds the number of bits of memory access unit of the memory (i.e., compression rate judging section 106 provides the rate of compression in connection with the storage capacity, i.e. number of bits of the memory 103, and the compressing section 107a or 107b which includes quantization control based on access width information compresses the data based upon the compressed rate information provided by compression rate judging section, see Figures 18, 24, 29, 30, 49-52, column 13, lines 16-44, column 14, lines 3-64, column 17, line 33 to column 19, line 13); wherein the compressor and the expander conduct compression and expansion, respectively, in accordance with a pixel difference prediction encoding system (see 107a of Figure 24, 107b of Figures 29 and 30, column 4); wherein the quantization controller (see 107b of Figures 29 and 30, 703a of Figures 50 and 51) controls quantization by preparing a plurality of quantizers (i.e., 121a-d of Figures 29 and 30; 703a of Figure 51) having quantization characteristics different from each other and a plurality of quantization characteristic tables, a quantization characteristic table (see 700 of Figure 50) being shared by the plurality of quantizers; wherein the compressor

and expander conduct compression and expansion, respectively, in accordance with an orthogonal translation encoding system (see column 4, column 9, lines 1-13); the compressor controls quantization characteristics used for quantizing the decoded image, based on control by the quantization controller (see Figures 29, 30, 50, 51); detecting a number of coded bits for every control unit of compression processing (i.e., 107a of Figures 18 and 24), and controlling the number of coded bits so that the number of coded bits is in conformity with the number of bits of a memory access unit of a memory (i.e., 103 of Figure 18) when the detected number of coded bits exceeds the number of bits of a memory access unit of the memory, wherein the step of controlling uses information from an external compressed data stream (see column 13, lines 16-44, column 13, line 61 to column 14, line 64, and 106 of Figure 18).

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohira et al as applied to claims 1-14 and 16-18 in the above paragraph (2), and further in view of Nakajima et al of record (6,243,421).

Ohira et al discloses substantially the same moving picture decoding method and apparatus as above, but does not particularly disclose the compressor comprising a subtracter, a quantizer, an encoder, an inverse quantizer, an adder and a predictor, a prediction error obtained in the subtracter by subtraction operation between the decoded image and a predicted value from the predictor is supplied to the quantizer, under control of the quantization controller, the

quantizer quantizes the prediction error and supplies the quantized result to the encoder and the inverse quantizer, the encoder encodes an output from the quantizer and outputs the encoded result to the memory, and inverse quantizer and local decoding are conducted in the inverse quantization, the adder and the predictor, as claimed in claim 15. However, Nakajima et al discloses an apparatus for decoding coded video data with reduced memory size as shown in Figures 2 and 3, and teaches the conventional compression means comprising a subtracter (20 of Figure 3), a quantizer (21 of Figure 3), an encoder (22 of Figure 3), an inverse quantizer (25 of Figure 3), an adder (23 of Figure 3) and a predictor (24 of Figure 3), a prediction error (i.e., output of 20 of Figure 3) obtained in the subtracter by subtraction operation between the decoded image and a predicted value from the predictor is supplied to the quantizer, under control of the quantization controller, the quantizer (i.e., 21 of Figure 3) quantizes the prediction error and supplies the quantized result to the encoder (22 of Figure 3) and the inverse quantizer (25 of Figure 3), the encoder encodes an output from the quantizer and outputs the encoded result to the memory (i.e., 6 of Figure 2), and inverse quantization and local decoding are constructed in the inverse quantization, the adder, and the predictor (see Figure 3). Therefore, it would have been obvious to one of ordinary skill in the art, having the Ohira et al and Nakajima et al references in front of him/her and the general knowledge of video compression systems, would have had no difficulty in providing the compression means as shown in Figure 3 of Nakajima et al including all the components as claimed in place of the compression system 107a of Figure 18 of Ohira et al for the same well known video compression with quantization control purposes as claimed.

(10) Response to Argument

Regarding the appellants arguments at pages 8-10 of the Brief filed September 28, 2005 concerning in general that "... Among the limitations of Appellants' claims not shown or disclosed in Ohira is a memory access width controller that controls said quantization controller such that bit allocation is controlled in relation to a number of bits of the memory bus that accesses said memory ... The Examiner merely repeats the rejection set forth in the Office Action of September 24, 2003 ... This merely means that the image data is stored in a predetermined storage capacity on a frame basis. However, at no time does Ohira discuss the bus accessing the memory (the memory access unit) ... ", the Examiner wants to initially point out that the memory bus feature as argued is not even claimed. Secondly, it is submitted again that since compression rate judging section 106 of Figure 18 of Ohira provides the rate of compression in connection with the storage capacity, i.e. number of bits of the memory 103, and bit allocation control to the quantization controller is provided within 107a, sections 106 and 107a of Ohira provides the same access width controller that controls the quantization controller such that bit allocation is controlled in relation to a number of bits of a memory access unit of the memory, as claimed (see column 13, lines 16-44, column 14, lines 3-64, column 17, line 33 to column 19, line 13 of Ohira).

Regarding the appellants arguments at page 10 of the Brief filed September 28, 2005 concerning in general that "Ohira's storage capacity is described at column 13, line 20 et seq. refers to the capacity of the frame memory, not the width of the bus that accesses the memory ... In a case where the teaching of Ohira is used, the compression data rate is not altered because the frame memory capacity is the same 128 megabytes, even though a different data bus width is

employed. On the other hand, where the claimed invention is used, when the memory having a different data bus is employed, the data compression rate is altered ... In contrast, in the Ohira reference, the width of the access bus is never taken into account. As such, the Ohira reference fails to disclose Appellants' explicitly recited claims ...", the Examiner wants to point out again that such features as argued concerning the "width of the bus that access the memory" and "when the memory having a different data bus is employed, the data compression rate is altered" do not correspond or correlate with the claim language. Put simply, these features are not claimed.

The appellants argued at page 11 of the Brief filed September 28, 2005 disagreeing with the Examiner's position that the "memory access unit is equivalent to a storage capacity of the frame memory" and that the claimed memory access unit is equivalent to an entrance ramp of a parking garage and the storage memory disclosed by Ohira is equivalent to the parking garage accessed by the entrance ramp. The appellants' analogies are greatly appreciated but it is still that the storage capacity of the frame memory within Ohira provides the equivalent of "a memory access unit of the memory" as claimed.

Regarding the appellants' arguments at page 11 of the Brief filed September 28, 2005 concerning that "The Examiner asserted that the Z number of bits within the memory is equivalent to the bus accessing the memory. However, this is incorrect, as the bus accessing the memory can be any number of bits wide regardless of the size of the actual memory. Appellants respectfully submit that Ohira fails to consider the number of bits of the memory bus that accesses the memory in performing a decoding operation ...", the Examiner wants to point out again that such limitations as argued are not claimed.

Regarding the appellants' arguments at pages 11-12 of the Brief filed September 28, 2005 concerning that Ohira fails to disclose or suggest controlling bit allocation as a function of the number of bits of the memory access unit of the memory, and that Nakajima was not included to cure this deficiency, the Examiner wants to point out that such arguments have been addressed in the above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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12/2/05

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